1069-001

UNITED STATES PATENT APPLICATION FOR GRANT OF LETTERS PATENT

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CURRENT SENSOR FOR DC POWERED THREE PHASE MOTOR CONTROL SYSTEM

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CURRENT SENSOR FOR DC POWERED THREE PHASE MOTOR CONTROL SYSTEM

Field of the Invention

[0001] The present invention relates sensing the output current of a motor control system, and more particularly relates to sensing the output current of three phase inverters.

Background of the Invention

[0002] Figure 1 illustrates a basic three phase inverter 10. In general, the three phase inverter 10 includes a voltage regulator and isolation circuit 12 connected to the power lines of the power grid and providing isolation from the power grid. Optionally, the voltage regulator and isolation circuit 12 may provide voltage reduction and/or voltage regulation. The voltage regulator 12 generates a direct current (DC) positive supply voltage (+BUS) that is referenced to earth ground (GND). Three "legs" of the three phase inverter 10 are connected between the positive supply voltage (+BUS) and ground (GND). Each of the legs operates to provide one of the three motor currents (I_{M1}, I_{M2}, I_{M3}). Transistors 14 and 16 from the first leg, transistors 18 and 20 form the second leg, and transistors 22 and 24 form the third leg. Each of the transistors 14-24 are controlled by a switching driver 26 such that the three phase inverter 10 generates the three motor currents (I_{M1}, I_{M2}, I_{M3}) that are used to drive a three phase motor.

[0003] In order to properly control a three phase motor, it is desirable to sense, or monitor, one or more of the motor currents (I_{M1}, I_{M2}, I_{M3}). In reality, once two of the three motors currents are known, the third motor current can be determined based on Kirchoff's current law which states that the sum of all current flowing into a node is zero, as is well known in the art. Sensing the motor currents with resistors is typically done in one of four ways. A first method places a single resistor between transistors 16, 20, and 24 and ground (GND), thereby sensing one or more of the motor currents. Although simple, this method does not provide enough information to determine each of the motor currents, and is therefore not suitable for high performance motor control.

[0004] A second method inserts a first sense resistors between one of the transistors 16, 20, 24 and ground (GND) and a second sense resistor between another of the transistors 16, 20, 24 and ground (GND). However, the motor current only flows in the sense resistors when the respective transistor 16, 20, or 24 is on. Therefore, sampling or estimation techniques must be used, which increases complexity and noise.

[0005] A third method inserts a first sense resistor in series with one of the three motor phases and a second sense resistor in series with a second of the three motor phases, such that one of the three motor currents (I_{M1}, I_{M2}, I_{M3}) follows directly through each of the sense resistors. Although this method provides good dynamic control of the motor, a small differential voltage from the sense resistors must be separated from a large AC common mode voltage due to the switching of the transistors 14-24. Circuits capable of rejecting the large AC common mode voltage are relatively expensive and/or large, and are thus less suited for small volume, high performance, motor drives.

[0006] A fourth method uses two upper and two lower sense resistors. For example, a first upper sense resistor is placed between transistor 14 and the positive supply voltage (+BUS), and a corresponding first lower sense resistor is placed between the transistor 16 and ground (GND). A second upper sense resistor is placed between the transistor 18 and the positive supply voltage (+BUS), and a corresponding second lower sense resistor is placed between the transistor 20 and ground (GND). The upper sense resistors are used to sense the motor currents (I_{M1}, I_{M2}) when respectively transistors 14 and 18 are active, and the lower sense resistors are used to sense the motor currents (I_{M1}, I_{M2}) when respectively transistors 16 and 20 are active. In principal, the sum of the currents through the upper and lower sense resistors in each leg is a continuous output current corresponding to the motor currents. In practice, outputs of the upper sense resistors must be amplified and differentially shifted down to ground where the common mode is rejected and the output of the lower sense resistors are added. Commonly used level shifters are a current mirror or a common base amplifier built with high voltage transistors. These transistors are temperature sensitive. For example, the gain and base to emitter voltage of the transistors varies with temperature.

Thus, an offset is introduced into the output signal that varies with temperature. Further, the offset can be a substantial fraction of the maximum sensed signal.

[0007] Thus, there remains a need for a system for sensing one or more motors currents from a three phase inverter that avoids the problems of the previous systems, including those described above.

Summary of the Invention

[0008] The present invention provides a system for sensing one or more motor currents generated by a three phase inverter. To sense a first motor current, a first sense resistor is coupled between a first transistor of the three phase inverter and a supply voltage, and a second sense resistor is coupled between a second transistor of the three phase inverter and ground. Circuitry coupled to the first and second sense resistors generates an upper and a lower current. When the first transistor is active and the second transistor is inactive, the upper current is essentially proportional to the sum of a first reference voltage and a voltage across the first sense resistor, and the lower current is essentially proportional to a second reference voltage. When the first transistor is inactive and the second transistor is active, the upper current is essentially proportional to the first reference voltage, and the lower current is essentially proportional to the sum of the second reference voltage and a voltage across the second sense resistor. Based on the difference of the upper and lower currents, the circuitry provides a first output current that is proportional to the first motor current.

[0009] In one embodiment, the first output current is digitized by an analog-to-digital (A/D) tracking converter, such as a delta sigma converter. In another embodiment, the system includes second circuitry adapted to sense a second motor current of the three phase inverter and that operates essentially the same as the circuitry described above. In yet another embodiment, the system includes a bias supply circuit that generates the reference voltages, which are essentially the same voltage. Preferably, the bias supply circuit generates each of the reference voltages from a single voltage source.

[0010] Those skilled in the art will appreciate the scope of the present invention and realize additional aspects thereof after reading the following

detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawings

[0011] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the invention, and together with the description serve to explain the principles of the invention.

[0012] Figure 1 illustrates a basic three phase inverter in the prior art;

[0013] Figure 2 illustrates a system for continuously sensing a motor current from a three phase inverter according to one embodiment of the present invention;

[0014] Figure 3 illustrates one embodiment of a bias supply circuit included in the system of Figure 2 according to one embodiment of the present invention;

[0015] Figure 4 illustrates one embodiment of an analog-to-digital (A/D) tracking converter included in the system of Figure 2 according to one embodiment of the present invention;

[0016] Figure 5 illustrates the system of Figure 2 further including filtering circuitry according to another embodiment of the present invention; and

[0017] Figure 6 illustrates a system for sensing two motor currents from a three phase inverter according to another embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0018] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the invention and illustrate the best mode of practicing the invention. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the invention and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0019] The description of the present invention begins at Figure 2 where a system 28 is illustrated for sensing one of three output currents of a three

phase inverter according to the present invention. In general, the system 28 includes first and second sensing resistors 30 and 32, respectively, each having a resistance value R_0. The first sensing resistor 30 is coupled between the positive supply bus (+ BUS) and a first switching transistor 34. The second sensing resistor 32 is coupled between a second switching transistor 36 and ground. The first and second switching transistors 34 and 36 form one leg 38 of a three phase inverter. For simplicity, the entire three phase inverter is not illustrated since it is well known in the art. An example of a three phase inverter is described in U.S. Patent No. 4,357,655 and is incorporated herein by reference in its entirety.

[0020] An upper amplifier 40 and an upper transistor 42 are connected as shown. The upper amplifier 40 and the upper transistor 42 operate as a voltage follower. Preferably, the upper transistor 42 is an P-channel field effect transistor (FET), but should not be limited as such. The upper amplifier 40 and the upper transistor 42 operate to provide a first fixed voltage (V_1) to an upper resistor 44 at node A, where the first fixed voltage (V_1) is provided by a bias supply circuit 46. In the embodiment of Figure 2, the first fixed voltage (V_1) is the negative terminal of a first voltage source 48. Similarly, a lower amplifier 50 and a lower transistor 52 operate to provide a second fixed voltage (V_2) to a lower resistor 54 at node B. The second fixed voltage (V_2) is provided by the bias supply circuit 46; and, in the embodiment of Figure 2, the second fixed voltage (V_2) is a voltage V_R from a second voltage source 56. Preferably, the lower transistor 52 is a N-channel field effect transistor (FET), but should not be limited as such. An analog-to-digital (A/D) tracking converter 58 is connected to node C and operates to digitize an output current (I_{OUT}), thereby generating a digital representation of the output current (DIGITIZED I_{OUT}). The output current (I_{OUT}) is directly proportional to the motor current (I_M) supplied by the leg 38 of the three phase inverter.

[0021] In the embodiment of Figure 2, each of the upper and lower resistors 44 and 54 have a resistance value of R_1, and the resistance R_0 of the first and second sensing resistors 30 and 32 is small compared to the resistance R_1. For example, the resistance R_0 may be 5 milliohms. Preferably, the voltage V_R is larger than the maximum voltage that will appear across the first and second sensing resistors 30 and 32 at maximum motor

current (I_M) such that the upper and lower transistors 42 and 52 operate linearly and act as current sources.

[0022] In operation, the switching transistors 34 and 36 are alternately activated. First we, consider that the second switching transistor 36 is active and the first switching transistor 34 is deactivated. Thus, the motor current (I_M) from the leg 38 of the three phase inverter can be defined as flowing from ground through the second switching transistor 36, as illustrated by dashed line. Thus, the current through the lower resistor 54 can be defined as:

$$I_{LOWER} = \frac{V_R}{R_1} + \frac{R_0 I_M}{R_1},$$

where V_R is the reference voltage supplied by the second voltage source 56 and that is provided at node B, R_1 is the resistance value of the lower resistor 54, R_0 is the resistance value of the second sensing resistor 32, and I_M is the output current of the leg 38 of the three phase inverter. Further, since the resistance R_0 of the first sensing resistor 30 is small compared to the resistance R_1 of the upper resistor 44, the current through the upper resistor 44 can be defined as:

$$I_{UPPER} = \frac{V_R}{R_1},$$

where V_R is the reference voltage supplied by the first voltage source 48 and R_1 is the resistance value of the upper resistor 44.

Thus, according to Kirchoff's current law, the output current (I_{OUT}) is:

$$I_{OUT} = I_{LOWER} - I_{UPPER} = \left(\frac{V_R}{R_1} + \frac{R_0 I_M}{R_1}\right) - \frac{V_R}{R_1} = \frac{R_0 I_M}{R_1}.$$

[0023] Now we consider when the first switching transistor 34 is active and the second switching transistor 36 is deactivated. Thus, the output current (I_M) of the leg 38 of the three phase inverter can be defined as flowing from the positive supply bus (+ BUS) through the first switching transistor 34, as illustrated by the solid line. Thus, the current through the upper resistor 44 can be defined as:

$$I_{UPPER} = \frac{V_R}{R_1} - \frac{R_0 I_M}{R_1},$$

where V_R is the reference voltage supplied by the first supply voltage 48, R_1 is the resistance value of the upper resistor 44, R_0 is the resistance value of the first sensing resistor 30, and I_M is the output current of the leg 38 of the three phase inverter. Further, since the resistance R_0 of the second sensing resistor 32 is small compared to the resistance R_1 of the lower resistor 54, the current through the lower resistor 54 can be defined as:

$$I_{LOWER} = \frac{V_R}{R_1},$$

where V_R is the reference voltage supplied by the second voltage source 56 and that is provided at node B and R_1 is the resistance value of the lower resistor 54. Thus, according to Kirchoff's current law, the output current (I_{OUT}) is:

$$I_{OUT} = I_{LOWER} - I_{UPPER} = \frac{V_R}{R_1} - \left(\frac{V_R}{R_1} - \frac{R_0 I_M}{R_1}\right) = \frac{R_0 I_M}{R_1}.$$

Therefore, the system 28 of the present invention provides the output current (I_{OUT}) that is a continuous signal and for all states of the first and second transistors 34 and 36 is defined by the equation:

$$I_{OUT} = \frac{R_0 I_M}{R_1}.$$

It should also be noted that when the current motor (I_M) from the leg 38 of the three phase inverter changes polarity (flows into the leg 38 rather than out of the leg 38), the polarity of the output current (I_{OUT}) will also change, where the output current (I_{OUT}) will flow into rather than out of the A/D tracking converter 58.

[0024] In general, the system 28 of Figure 2 produces the digitized output current (DIGITIZED I_{OUT}) that is proportional to the motor current (I_M) produced by one leg 38 of a three phase inverter. The digitized output current (DIGITIZED I_{OUT}) is a continuous representation of the motor current (I_M) that is independent of the switching of the transistors 34 and 36 of the leg 38 of the three phase inverter. Further, upon changing the polarity of the motor current (I_M), the polarity of the output current (I_{OUT}) also changes. In addition, due to the upper and lower symmetry of the system 28 and the fact that the upper and lower currents (I_{UPPER}, I_{LOWER}) are each generated based on the

reference voltage V_R, the system 28 does not require level shifting circuitry and the output current (I_{OUT}) can be directly digitized by the A/D tracking converter 58.

[0025] Figure 3 illustrates one embodiment of the bias supply circuit 46 that may be used to provide the bias supply circuit 46 for the system 28 illustrated in Figure 2. In this embodiment, a single voltage source 60 is used to generate two separate reference voltages (V_R). In general, the bias supply circuit 46 includes an amplifier 62 and transistor 64 connected as shown and operating as a voltage follower. The amplifier 62 and the transistor 64 operate to provide the voltage V_R from the voltage source 60 to resistor 66 at node D, thereby generating the voltage V_R across the resistor 66. Further, by generating the voltage V_R across the resistor 66, a current is induced in resistor 68. Since the resistors 66 and 68 have the same resistance value R_2, the voltage V_R is also generated across the resistor 68. The capacitor 70 operates to reduce noise. The bias supply circuit 46 may also include a second transistor 72, resistor 74, and diode 76 arranged as shown to generate a negative supply voltage ($-V_S$) used by the upper amplifier 38 (Figure 1). In one embodiment, the transistor 72 is a bipolar junction transistor (BJT) and the diode 76 is a zener diode.

[0026] The benefit of the bias supply circuit 46 of Figure 3 is that two voltage references V_R are created from a single voltage source 60. In doing so, the offset of the output current (I_{OUT}) is stable. Typically, one source of offset is variation in bias supply circuit 46 due to temperature. By generating both voltage references V_R from a single voltage source 60, both of the voltage references V_R have the same variations due to temperature. Referring to the equations for I_{OUT} above, since the variations for the reference voltages V_R are the same, the V_R terms will cancel. Thus, as long as the voltage references V_R are substantially the same, the output current will not have an offset due to variations in temperature. It should be noted that the embodiment of the bias supply circuit of Figure 3 is an exemplary embodiment. The bias supply circuit 46 can be any circuit that generates separate reference voltages V_R that are substantially the same voltage over temperature.

[0027] Other sources of offset and scale factor drift in the output current (I_{OUT}) may exist. However, these offsets are stable and the scale factor is stable due to the tolerances and stability of the resistors 30, 32, 44, and 54 and the stable offset of amplifiers 40 and 50. Use of MOSFET's for transistors 42 and 52 and the inclusion of the transistors 42 and 52 inside the feedback loops of amplifiers 40 and 50, as shown, insures that the transistors 42 and 52 contribute no significant drift in the offset or scale factor. Since stable offsets do not vary with time or temperature, the offset can be determined when both of the transistors 34 and 36 (Figure 2) are deactivated, where the value of output current (I_{OUT}) is essentially the offset. Once the offset is determined, the offset can be subtracted from future values of the output signal (I_{OUT}).

[0028] Figure 4 illustrates one embodiment of the A/D tracking converter that may be used as the A/D tracking converter 58 in Figure 2. In general, the converter 58 includes an amplifier 78, logic 80, resistor 82, and capacitor 84 arranged as shown and operating as a delta sigma converter. In one embodiment, the logic 80 is a flip/flop. In operation, the output signal (I_{OUT}) is received by an inverting input (-) of the amplifier 78. The digitized output signal (DIGITIZED I_{OUT}) from the logic 80 is fed back into the inverting input of the amplifier 78 such that it is subtracted from the output signal (I_{OUT}). The difference is integrated by the amplifier 78 and digitized by the logic 80.

[0029] Figure 5 illustrates another embodiment of the system 28. This embodiment is similar to the embodiment illustrated in Figure 2 and further includes noise filtering. More particularly, resistor 86 and capacitor 88 protect the upper transistor 42 from any high frequency ring voltage that may exist between the positive supply bus (+ BUS) and ground, and capacitor 96 and resistor 86 protect the lower transistor 52. Further, the voltage across the current sense resistors 30 and 32 can include fast, high amplitude noise spikes caused by the inductance of the sensing resistors 30 and 32 and reverse recovery currents in the leg 38 of the three phase inverter. The noise spikes can be filtered so the output current (I_{OUT}) does not clip. To accomplish this filtering, the upper resistor 44 is split into two resistors 44A and 44B, and capacitor 90 is connected to the positive supply bus (+ BUS) as shown. Similarly, the lower resistor 54 is split into two resistors 54A and 54B,

and capacitor 92 is connected to ground as shown. Resistor 94 and capacitor 96 may be added to filter high frequencies from the A/D tracking converter 58.

[0030] Figure 6 illustrates another embodiment of the system 28 that senses two motor currents (I_{M1} and I_{M2}) from two legs of a three phase inverter. Based on the two motor currents (I_{M1} and I_{M2}), the third motor current (I_{M3}) may be determined based on Kirchoff's current law. The legs of the three phase converter have been omitted for simplicity. In addition, the filtering circuitry of Figure 5 may be included in this embodiment, but have been omitted for simplicity.

[0031] The operation of the system 28 of this embodiment is essentially the same as the operation of the embodiments described above. To sense the second motor current (I_{M2}), the system 28 includes sensing resistor 98, amplifier 100, transistor 102, upper resistor 104, sensing resistor 106, amplifier 108, transistor 110, and lower resistor 112 connected as shown. The operation of the sensing resistor 98, the amplifier 100, the transistor 102, and the upper resistor 104 is similar to the operation of the first sensing resistor 30, the upper amplifier 40, the upper transistor 42 and the upper resistor 44 described above. The operation of the sensing resistor 106, the amplifier 108, the transistor 110, and the lower resistor 112 is similar to the operation of the second sensing resistor 32, the lower amplifier 50, the lower transistor 52 and the lower resistor 54 described above.

[0032] *Resistors 114-128 operate to reduce cross coupling between* sensing resistors 30 and 98 and between sensing resistors 32 and 106. Preferably, resistors 114, 118, 122, and 126 have a resistance value R_7 that is much larger than a resistance value R_8 of the resistors 116, 120, 124, and 128. To accommodate the used of the resistors 114-128, the voltage source 60 of the bias supply circuit 46 produces a voltage equal to $V_R(1+R_7/R_8)$. Thus, the bias supply circuit 46 generates the voltage V_R across the resistors 116, 120, 124, and 128, and the system 28 continues to operate as described above. Accordingly, the first output current (I_{OUTA}) corresponds to the first motor current and is defined by the equation:

$$I_{OUTA} = \frac{R_0 I_{M1}}{R_1},$$

and the second output current (I_{OUTB}) corresponds to the second motor current and is defined by the equation:

$$I_{OUTB} = \frac{R_0 I_{M2}}{R_1}.$$

By sensing two of the three motors currents supplied by the three phase inverter, the third motor current can be calculated using Kirchoff's current law. It should also be noted that each of the output currents I_{OUTA} and I_{OUTB} are preferably digitized by circuitry such as the A/D tracking converter 58. However, for simplicity, such conversion circuitry has been omitted from Figure 6.

[0033] The present invention provides substantial opportunity for variation without departing from the spirit or scope of the invention. For example, although Figure 6 illustrates a preferred embodiment of the system 28 for sensing two motor currents, the system 28 of Figure 1 could be used for each of two or more motor currents. As another example, although transistors 40 and 50 (Figures 2, 5, and 6), transistor 64 (Figures 3 and 6), and transistors 102 and 110 (Figure 6) have been illustrates and FETs, other types of transistors or current sources may be used and should be considered within the spirit and scope of the present invention. As yet another example, although one embodiment of the A/D tracking converter 56 is illustrated in Figure 4, there are numerous variations of the A/D tracking converter 56 that will be obvious to one of ordinary skill in the art and such variations should be considered within the spirit and scope of the present invention. As yet another example, the resistors 114-126 may optionally be included in the bias supply circuit 46.

[0034] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present invention. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.